ECS371 Review Questions

Name_____

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

1) Digital data can be processed and transmitted more efficiently and reliably than analog information. 1) _____

2) The decimal number system uses nine different digits. 2) _____

3) The binary number system uses just two digits. 3) _____

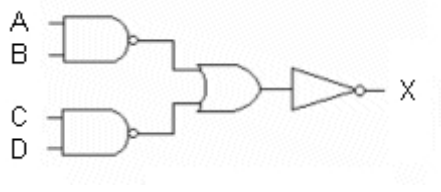
4) When the inputs to a 2-input AND gate are both HIGH, the output is HIGH. 4) _____

5) When the inputs to a 2-input AND gate are both LOW, the output is LOW. 5) _____

6) Boolean multiplication is symbolized by A + B. 6) _____

7) In Boolean algebra, $1 \cdot 0 = 0$. 7) _____

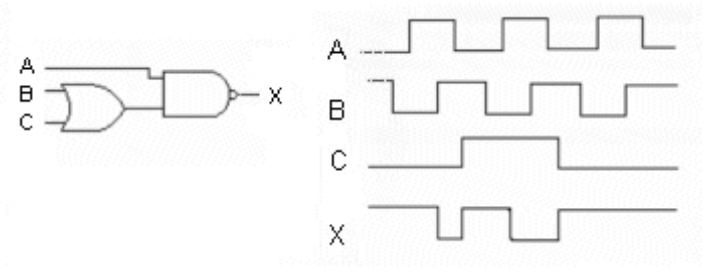
8) This circuit is an example of the implementation of AND-OR-INVERT logic. 8) _____



9) The Karnaugh map below represents the correct implementation of the expression, X = ACD + AB(CD + BC). 9) _____

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	0	0	0	0
$\overline{A}B$	0	0	1	1
AB	0	0	0	1
$A\overline{B}$	0	0	0	1

10) The waveforms are correct for the logic circuit shown. 10) _____



11) The look-ahead-carry adder is slower than the ripple-carry adder because it requires additional logic circuits. 11) _____

12) A demux basically reverses the function of a mux. 12) _____

13) A mux basically reverses the function of a demux. 13) _____

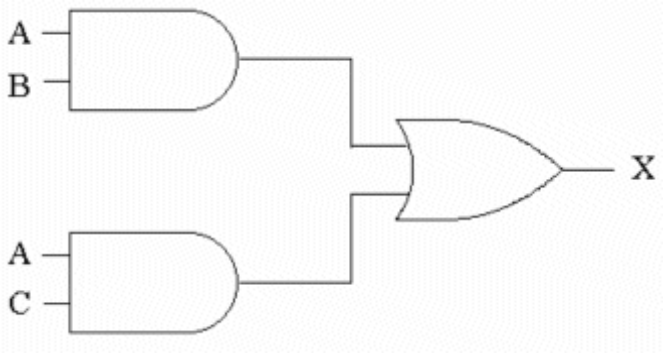


Figure 4-1

14) For the circuit in Figure 4-1, X = 0 whenever A = 0, regardless of the levels applied to inputs B and C. 14) _____

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

15) The largest single digit in the decimal number system is _____. 15) _____
A) 9 B) ∞ C) 1 D) 10

16) In the decimal value 4256, the weight of the numeral 2 is _____. 16) _____
A) 10^3 B) 10×2^2 C) 10^2 D) 200

17) How many binary digits are required to count to decimal 100? 17) _____
A) 7 B) 3 C) 2 D) 100

18) Decimal 42 is equivalent to binary _____. 18) _____
A) 01000010 B) 52 C) 101010 D) 2A

19) In binary systems the sign of a number is indicated by _____. 19) _____

A) placing a negative sign in front of the number
B) using a 0 (zero) bit in front of negative numbers
C) inverting the bits if the number is negative
D) including a sign bit along with the magnitude bits

20) When performing binary addition using the 2's complement method, an overflow can occur if _____. 20) _____

A) both numbers have the same sign
B) both numbers have the same magnitude
C) one number is negative and the other is positive
D) the second number is much greater than the first

21) This is the truth table for a(n) _____. 21) _____

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

A) OR gate B) AND gate C) NOR gate D) NAND gate

22) Which of these truth tables represents the Exclusive-NOR gate? 22) _____

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

(A)

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

(B)

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

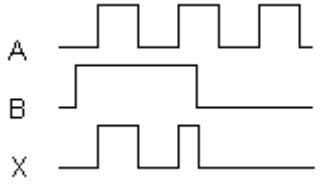
(C)

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(D)

A) (A) B) (B) C) (C) D) (D)

23) This is the timing diagram for a 2-input _____ gate. 23) _____



A) AND B) NAND C) OR D) Exclusive-OR

24) The difference between a PLA and a PAL is _____. 24) _____

A) the PAL has more possible product terms than the PLA
B) the PLA has a programmable OR plane and a programmable AND plane while the PAL only has a programmable AND plane
C) the PAL has a programmable OR plane and a programmable AND plane while the PLA only has a programmable AND plane
D) PALs and PLAs are the same thing.

25) The expression for a 3-input NOR gate is _____. 25) _____

A) $\overline{A + B + C}$ B) A/B/C C) $A \cdot B \cdot C$ D) $\overline{A} + \overline{B} + \overline{C}$

26) Which of the examples below expresses the associative law of addition? 26) _____

A) A + (B + C) = A + (BC) B) A(BC) = (AB) + C

C) ABC = A + B + C D) A + (B + C) = (A + B) + C

27) Which of the examples below expresses the distributive law? 27) _____

A) (A + B) + C = A + (B + C) B) A(BC) = (AB) + C

C) A(B + C) = AB + AC D) A + (B + C) = AB + AC

28) Which of the following is a form of DeMorgan's theorem? 28) _____

A) $\overline{X + Y} = \overline{X} + \overline{Y}$ B) $\overline{XY} = \overline{X} + \overline{Y}$ C) X(I) = X D) X + 0 = 0

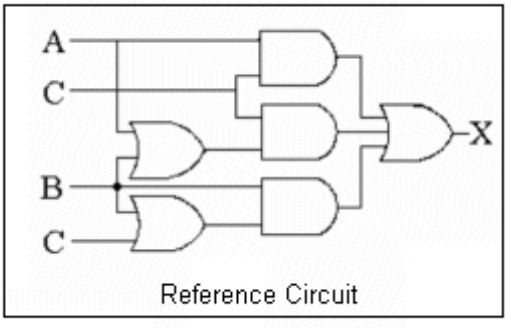
29) Which of the following expressions is in the sum-of-products form? 29) _____

A) (A + B)(C + D) B) (AB)(CD) C) AB + CD D) AB(CD)

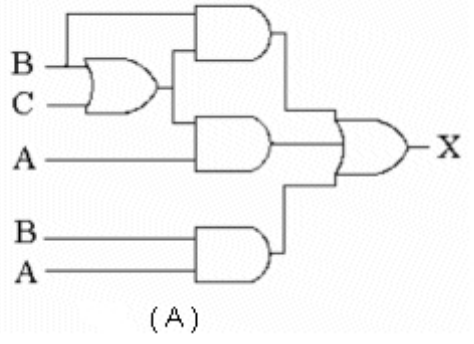
30) Which of the following expressions is in the product-of sums form? 30) _____

A) AB(CD) B) AB + CD C) (A + B)(C + D) D) (AB)(CD)

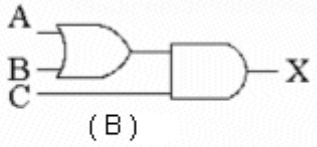
31) Which of the circuits below is equivalent to the Reference Circuit? 31) _____



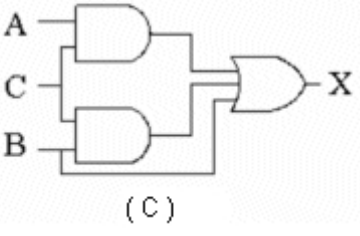
Reference Circuit



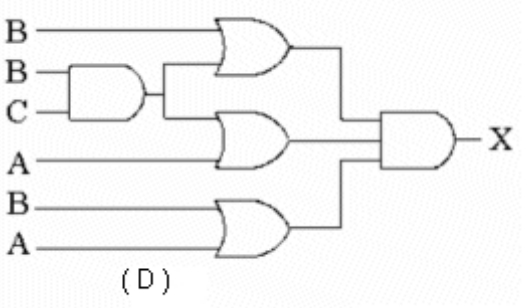
(A)



(B)



(C)



(D)

A) Figure (A) B) Figure (B) C) Figure (C) D) Figure (D)

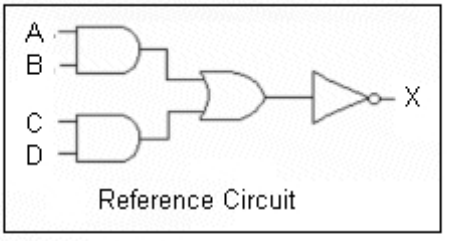
32) Which statement below best describes a Karnaugh map? 32) _____

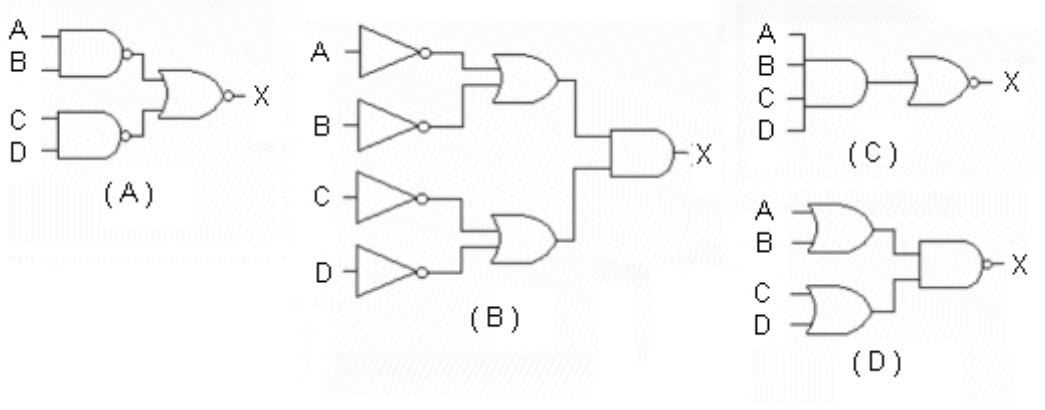
A) The Karnaugh map eliminates the need for using NAND and NOR gates.
B) A Karnaugh map can be used to replace Boolean rules.
C) Variable complements can be eliminated by using Karnaugh maps.
D) Karnaugh maps provide a cookbook approach to simplifying Boolean expressions.

33) Occasionally, a particular logic expression will be of no consequence in the operation of a circuit, such as in a BCD-to-decimal converter. These result in _____ terms in the K-map and can be treated as either _____ or _____, in order to _____ the resulting term. 33) _____

A) duplicate, 1s, 0s, verify
B) spurious, ANDs, ORs, eliminate
C) don't care, 1s, 0s, simplify
D) spurious, 1s, 0s, simplify

34) Which figure is the equivalent of the Reference Circuit? 34) _____





A) Figure (A) B) Figure (B) C) Figure (C) D) Figure (D)

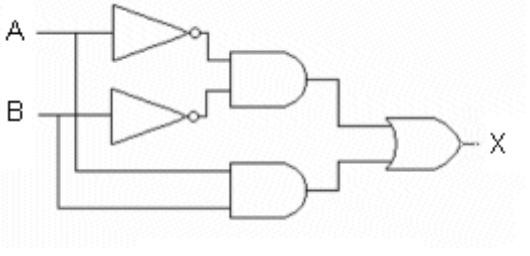


Figure 5-1

35) What type of logic circuit is represented by Figure 5-1? 35) _____

A) XAND B) XNOR C) XOR D) XNAND

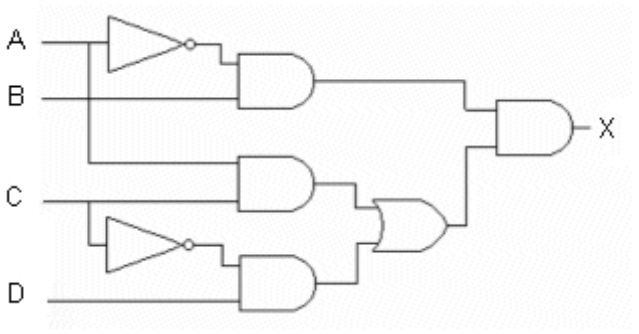


Figure 5-2

36) A correct logic expression for Figure 5-2 is _____. 36) _____

A) X = $A\overline{B}\overline{C}(\overline{C}BD)$ B) X = $(\overline{A}B)(AC + \overline{C}D)$

C) X = $(\overline{A}B)(A\overline{C}CD)$ D) X = $\overline{A}BC + A\overline{C}D$

37) The NAND gate is referred to as a "universal" gate, because it _____. 37) _____

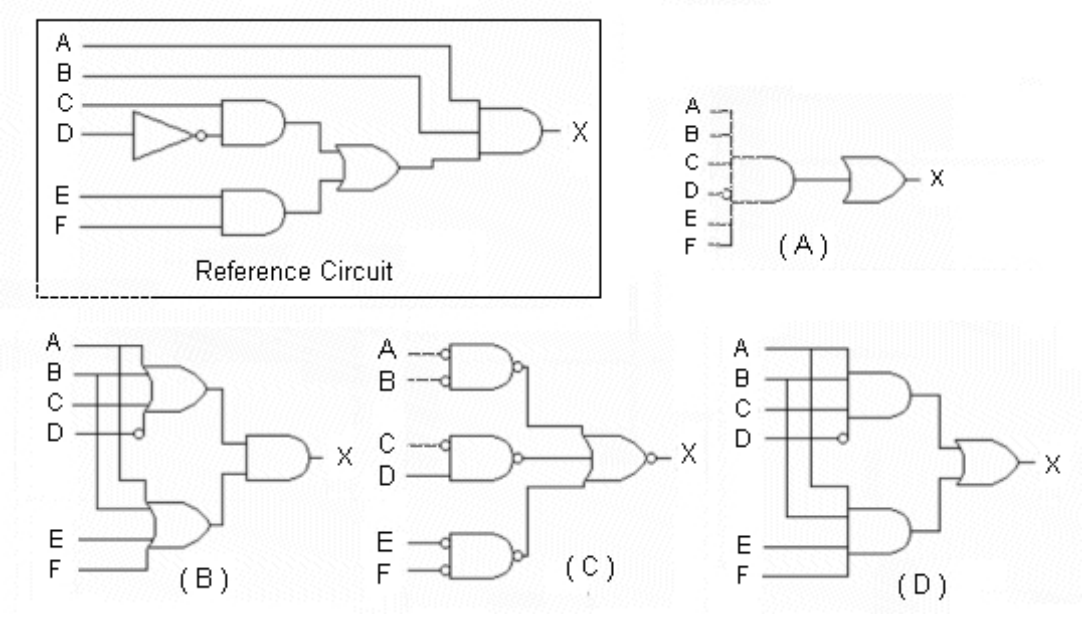
A) is used in all the countries of the world

B) can be found in almost all digital circuits

C) can be used to build all the other types of gates

D) was the first gate to be integrated

38) Which circuit is the sum-of-products equivalent of the Reference Circuit? 38) _____



A) Figure(A) B) Figure (B) C) Figure (C) D) Figure (D)

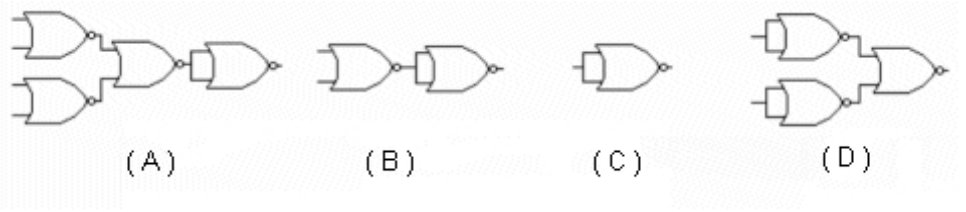


Figure 5-4

39) Which circuit in Figure 5-4 represents the NOR implementation of an OR gate? 39) _____
A) Figure (A) B) Figure (B) C) Figure (C) D) Figure (D)

40) Which circuit in Figure 5-4 represents the NOR implementation of an AND gate? 40) _____
A) Figure (A) B) Figure (B) C) Figure (C) D) Figure (D)

41) Which circuit in Figure 5-4 represents the NOR implementation of an inverter? 41) _____
A) Figure (A) B) Figure (B) C) Figure (C) D) Figure (D)

42) The carry output of a half-adder circuit can be expressed as _____. 42) _____
A) $C_{out} = A + B$ B) $C_{out} = A \oplus B$ C) $C_{out} = AB$ D) None of these

43) The expression $A \oplus B$ represents _____. 43) _____
A) The summing output of a half-adder B) The summing output of a full-adder
C) The carry output of a full-adder D) The carry output of a half-adder

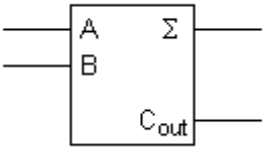


Figure 6-1

44) The symbol in Figure 6-1 represents a(n) _____. 44) _____
A) Half-adder B) Full-adder C) AND function D) PLD

45) Referring to the symbol in Figure 6-1, which set of outputs is very unlikely to ever occur? 45) _____
A) $\Sigma = 1, C_{out} = 0$ B) $\Sigma = 0, C_{out} = 0$ C) $\Sigma = 1, C_{out} = 1$ D) $\Sigma = 0, C_{out} = 1$

46) What is the major difference between half-adders and full-adders? 46) _____
A) Full-adders can handle double digit numbers.
B) Half-adders can only handle single digit numbers.
C) Full-adders have a carry input capability.
D) Nothing basically; full-adders are made up of two half-adders.

47) Which of the following is correct for full-adders? 47) _____
A) Full-adders are used to make half-adders.
B) Full-adders are limited to two inputs, since there are only two binary digits.
C) Full-adders have the capability of directly adding decimal numbers.
D) In a parallel full-adder, the first stage may be a half-adder.

48) The expression $(A \oplus B) \oplus C_{in}$ represents _____. 48) _____

A) The carry output of a full-adder
B) The summing output of a half-adder
C) The carry output of a half-adder
D) The summing output of a full-adder

49) The expression $AB + (A \oplus B)C_{in}$ represents _____. 49) _____

A) The summing output of a full-adder
B) The carry output of a full-adder
C) The carry output of a half-adder
D) The summing output of a half-adder

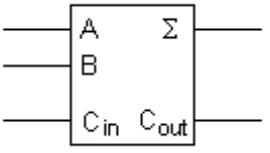


Figure 6-2

50) Refer to the symbol in Figure 6-2. What are the output when A = 1, B = 1, C_{in} = 1? 50) _____

A) Σ =1, C_{out} = 1 B) Σ = 1, C_{out} = 0 C) Σ = 0, C_{out} = 1 D) Σ = 0, C_{out} = 0

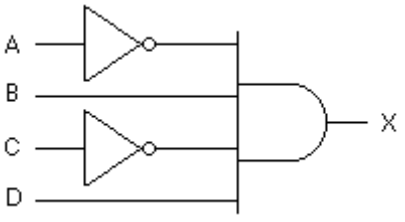
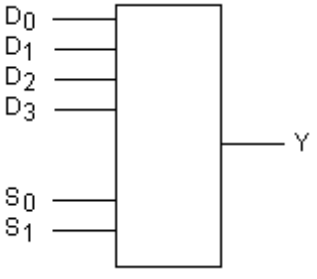


Figure 6-3

51) The output of the decoder in Figure 6-3 will be 1 only when _____. 51) _____

A) A = 0, B = 0, C= 0, D = 0
B) A = 1, B = 1, C= 1, D = 1
C) A = 1, B = 0, C= 1, D = 0
D) A = 0, B = 1, C= 0, D = 1

52) The circuit below is most likely a _____. 52) _____

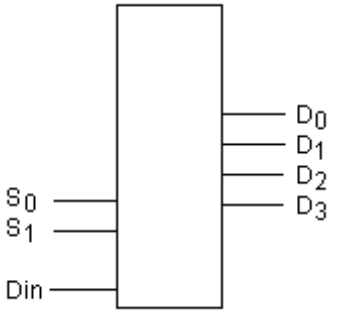


A) demultiplexer B) full-adder C) multiplexer D) comparator

53) A multiplexer with four select, or address, lines can select one of _____ inputs. 53) _____

A) 7 B) 3 C) 15 D) 16

54) The circuit below is most likely a _____. 54) _____



A) full-adder B) multiplexer C) demultiplexer D) comparator